IN THE CLAIMS

Please amend Claim 2 as indicated below. Please cancel Claims 3 to 10 without prejudice. A complete listing of the claims is provided herewith.

1. (Original) A CMOS circuit comprising:

a first gate reference voltage

a first bias current source; and

a device having its gate coupled to the first gate reference voltage, the device coupled in series with the first bias current source and having a gate size and structure to enhance its sensitivity to process, voltage and temperature variations thereby compensating the first bias current source for same.

2. (Currently Amended) A CMOS circuit as claimed in Claim 1, wherein the size of the gate is a relatively short length relative to other gates in the CMOS circuit.

3-10. (Canceled)